In the Claims:

1. (Currently Amended) A semiconductor integrated circuit, the integrated circuit comprising:

a silicon substrate having a substantially planar top substrate surface;

a silicon epitaxial layer having a lower resistivity than the resistivity of said silicon substrate, the epitaxial layer having a substantially planar lower epitaxial surface, the epitaxial layer being formed upon the top substrate surface so that the lower epitaxial surface and the top substrate surface are adjacent;

a first and a second circuit disposed ~~section formed~~ in said silicon epitaxial layer forming respectively a first and a second circuit section, each circuit ~~section~~ spaced apart from the top substrate surface by a respective portion of the silicon epitaxial layer; and

a device isolation region disposed between the first and second circuit sections to electrically separate the first and second circuit sections, the device isolation region extending from a top surface of each of the first and second circuit sections to an inner part of the silicon epitaxial layer;~~projecting from said silicon substrate up to a top surface of each of said first and second circuit sections between said first and second circuit sections;~~

wherein the portions of the epitaxial layer under both the first and second circuits are in contact with the substrate; and~~substrate.~~

wherein the device isolation region is spaced apart from the first and second circuit by respective portions of the silicon epitaxial layer.

2. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein the resistivity of said silicon substrate is between 20 and 100 times the resistivity of said silicon epitaxial layer.

3. (Previously Presented) The semiconductor integrated circuit according to Claim 2, wherein the resistivity of said silicon substrate is between 50 and 100 times the resistivity of said silicon epitaxial layer.

4. (Canceled).

5. (Currently Amended) The semiconductor integrated circuit according to Claim 1, wherein ~~a digital circuit is formed on said first circuit section, and an analog circuit is formed on said second circuit section.~~ the first circuit comprises a digital circuit and the second circuit comprises an analog circuit.

6-10. (Cancelled)

11. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon epitaxial layer is a single layer.

12. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon epitaxial layer is a p-type bulk epitaxial layer.

13. (Previously Presented) The semiconductor integrated circuit according to Claim 12, wherein said silicon substrate comprises a p-type bulk substrate.

14. (Previously Presented) The semiconductor integrated circuit according to Claim 13, wherein a first impurity concentration of the p-type bulk substrate is one-hundredth or less a second impurity concentration of the p-type bulk epitaxial layer.

15. (Previously Presented) The semiconductor integrated circuit according to Claim 13, wherein said silicon substrate has a thickness of 0.7mm and a resistivity of 1000 Ohm – cm.

16. (Cancelled)

17. (Previously Presented) The semiconductor integrated circuit according to Claim 12, wherein said silicon epitaxial layer has a thickness of 5 micrometers and a resistivity of 10 Ohm – cm.

18. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon substrate and said silicon epitaxial layer are of the same conductivity type.

19. (new) A semiconductor integrated circuit, the integrated circuit comprising:

a silicon substrate having a substantially planar top substrate surface;

a first circuit section formed directly on the substrate and comprising a first silicon epitaxial layer portion and a first circuit, the first circuit formed in the first epitaxial layer and comprising a portion of a top surface of the first circuit section;

a second circuit section formed directly on the substrate and comprising a second silicon epitaxial layer portion and a second circuit, the second circuit formed in the first epitaxial layer and comprising a portion of a top surface of the second circuit section;

a device isolation region disposed between the first and second circuit sections, the device isolation region extending from the top surface of each of the first and second circuit sections to an inner part of the silicon epitaxial layer; and

wherein the device isolation region is spaced apart from the first and second circuit by respective silicon epitaxial layer portions.

20. (new) The semiconductor integrated circuit of claim 19, wherein the first circuit comprises a digital circuit and the second circuit comprises an analog circuit.

21. (new) The semiconductor integrated circuit of claim 19, wherein the device isolation region is disposed directly adjacent to each of the first and second circuit sections.

22. (new) The semiconductor integrated circuit of claim 19, wherein the device isolation region is disposed entirely between side edges of the first and second circuit sections.

23. (new) The semiconductor integrated circuit of claim 1, wherein the device isolation region is disposed directly adjacent to each of the first and second circuit sections.

24. (new) The semiconductor integrated circuit of claim 1, wherein the device isolation region is disposed entirely between side edges of the first and second circuit sections.

25. (new) The semiconductor integrated circuit of claim 1, wherein the first and the second circuit is a diffusion layer of the same conductive type as the silicon expitaxial layer, and

wherein an impurity concentration of the diffusion layer is higher than that of the silicon epitaxial layer.

26. (new) An intermediate semiconductor integrated circuit, the intermediate integrated circuit comprising:

a silicon substrate having a substantially planar top substrate surface;

a silicon epitaxial layer having a lower resistivity than the resistivity of said silicon substrate, the epitaxial layer having a substantially planar lower epitaxial surface, the epitaxial layer being formed upon the top substrate surface so that the lower epitaxial surface and the top substrate surface are adjacent;

a device isolation region disposed between a first and second portion of the silicon epitaxial layer to electrically separate a first and second circuit sections, the device isolation region extending from a top surface of each of the first and second portions to an inner part of the silicon epitaxial layer;

wherein the portions of the epitaxial layer under both the first and second portions are in contact with the substrate; and

wherein the device isolation region is spaced apart from wells in the first and second portions by end-portions of the silicon epitaxial layer.